all. The claims are now in condition for allowance and Applicant respectfully requests withdrawal of the rejections based on 35 U.S.C. § 112, second paragraph, and allowance of independent claims 6, 20 and 27 as well as all claims dependent therefrom.

CLAIM REJECTIONS UNDER 35 U.S.C. §§ 102 and 103

Claims 6, 7 and 20-31 are rejected under 35 U.S.C. §103(a). More specifically, the rejection as stated in the Office Action mailed 3/13/01 was based on a reference, Grider et. al. Specifically, the rejection relies on an assertion that, "it would have been obvious within the scope of one of ordinary skill in the art to employ a dosage higher than 10exp14/cm with the expectation that the disclosed concomitant and disadvantages would be obtained, namely gate oxide degradation." Office Action of 3/13/01 at pg. 4. To support this statement, the Office Action points to "the expectation of obtaining disadvantages" from the cited art. Applicant fails to understand how "the expectation of obtaining disadvantages" or disclosure of "concomitant and disadvantages" from the cited art renders Applicant's claims obvious. As Examiner refused to talk to Applicant by telephone about this, Applicant kindly requests that the Examiner restate the argument.

Independent claim 6 provides, *inter alia*, introducing halogen-containing impurities into a semiconductor substrate to form a higher halogen concentration in a first region as compared to a second region. Introducing the halogen-containing impurities comprises introduction of halogen-containing impurities into both the first and second regions at different concentrations. Based on this differential concentration in both the first and second regions, a single oxidation step is performed to "*simultaneously* form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region . . ."

Grider et al. does ***not*** disclose, teach, or suggest such a limitation. More specifically, Grider et al. does not disclose creating two regions each doped with halogen-containing impurities, which control a single oxidation step resulting in different oxide thicknesses being simultaneously formed over the two regions.

In response, the Office Action or 3/13/01 states that "Grider et al. teaches that a second introduction of halogen species may be performed in a different region to achieve an even greater thickness differential between the thin and thick gate oxides." Office Action of

3/13/01 at pg. 4. However, this mischaracterizes Grider et al. In fact, Grider et al. states that "a second introduction of halogen species ...may be performed ***after oxidation*** to increase the oxide thickness." Grider et al. at col. 4, lns. 21-25. Thus, unlike Applicant's claim 6, Grider et al. fails to teach, disclose, or suggest formation of two different concentrations of halogen-containing impurities that result in differential oxide layer thickness from a single simultaneous oxidation step. Accordingly, Grider et al. fails to render Applicant's claim 6 obvious and Applicant respectfully requests withdrawal of this new rejection and allowance of claim 6 and all claims dependent therefrom.

Claims 2, 4, 5, 8 and 9 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Grider et al. (U.S. Patent No. 6,093,659). Claims 10 and 11-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2-9 and 20-28 above. Claims 6, 7 and 20-31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8 and 9 above. Applicant respectfully traverses the rejections with respect to independent claims 2, 6, 20, 24 and 27.

Claims 2, 4, 5, 8 and 9 are rejected as being anticipated by Grider et al. Applicant respectfully traverses the rejection with respect to independent claim 2 which includes, *inter alia*, "providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide thickness is desired, said first region ***directly adjacent*** said second region . . ." Grider et al. does not disclose, teach, or suggest providing the two regions ***directly adjacent*** to each other.

In direct contrast, "Grider et al. [only] teaches the two regions adjacent one another." Office Action of 3/13/01 at pg. 3. Specifically, Figure 4 of Grider et al. cited in the rejection clearly shows two regions (34) separated by an isolation structure (32). Grider et al. at fig. 4. Two regions (34) explicitly separated by an isolation structure (32) ***are not directly adjacent***. The rejection further relies on Grider et al. column 1, lines 30-38 and column 2, lines 30-36 to anticipate Applicant's directly adjacent limitation. Office Action of 3/13/01 at pg. 3. However, neither of the cited passages disclose, teach or suggest forming regions ***directly adjacent***. Rather, the cited passages provide only a general description of what is clearly illustrated in Figure 4.

Accordingly, Grider et al. fails to disclose, teach or suggest every element of Applicant's claim 2. Hence, for at least this reason, Applicant respectfully requests withdrawal of the rejection based on 35 U.S.C §102 and allowance of claim 2, as well as all claims dependent therefrom.

The advisory action asserts that this argument is overcome based on Grider et al., Column 1, lines 30-38. Specifically the cited reference states:

> "One prior art method for obtaining dual gate oxide thickness is called 'split-gate'. In one 'split gate' process, an initial oxide is grown followed by photolithographically masking areas where thick oxides are desired, then etching the grown oxide in areas where the thin oxide is required. The photo-resist is then removed via a clean-up process that may include ashing and a final oxidation is performed to grow the the thin oxide and anneal and slightly thicken the oxide already grown in the thick oxide areas."

This does not disclose forming two regions directly adjacent. Accordingly, it cannot render Applicant's claim anticipated as asserted in the Office and Advisory actions.

The Office Action rejects claims 20, 24 and 30 because, "it would be a matter of routine optimization within the teachings of Grider to determine a suitable implant energy and a suitable time, temperature and pressure, to achieve the halogen concentration regions formation step, and the oxide layers formation step, respectively." Office Action of 3/13/01 at pg. 4. Grider et al. discloses use of halogen-containing impurities only to ***retard*** oxidation. Grider at col. 1, lns. 65-67, col. 2, lns. 1-2, 52-53. Thus, adhering to the disclosure of, it would indeed ***not*** be routine to determine energy, time, temperature and pressure for introducing halogen-containing species to ***enhance*** oxidation. See e.g., Application at pg. 8, lns. 23-24. Thus, at best, the assertion promoted in the Office Action as routine, but not disclosed, taught or suggested, is ***not*** capable of instantaneous and unquestionable demonstration. Accordingly, Applicant respectfully traverses the assertion and either requests withdrawal of the assertion and allowance of claims 20, 24 and 30, along with all claims dependent therefrom or, in the alternative, a reference in support of the assertion. MPEP 2144.03. As previously discussed, the finality of the present Office Action should be removed due to the untimely and unsupported official notice.

Finally, added claim 32 is allowable for at least the aforementioned reasons.

PATENT

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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APPENDIX A

2. (As previously amended twice) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, said first region directly adjacent said second region;

introducing a halogen-containing impurities into an exposed surface of said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

forming a first memory gate electrode on said second oxide layer thickness, said second oxide layer thickness formed on said semiconductor substrate in a memory region.

4. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises an ion implantation.

5. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region and wherein said second region has substantially no halogen concentration therein.

6. (Four times amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region at a first concentration and introducing halogen-containing impurities into said second region at a second concentration, said first concentration greater than said second concentration, both said first and second concentrations formed of a dosage of said halogen-containing impurities greater than about 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2.

7. (As previously amended) The method of claim 6 wherein introducing said halogen-containing impurities comprises an ion implantation.

8. (As previously amended) The method of claim 2 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

D' cont

9. (As previously amended) The method of claim 2 wherein said semiconductor substrate also includes a third region where a third oxide layer thickness is desired, and wherein introducing said halogen-containing impurities also introduces halogen-containing impurities such that a different halogen concentration is formed in said third region than in said first region and in said second region.

10. (As previously amended) The method of claim 2 wherein said semiconductor device comprises a flash EEPROM semiconductor device.

11. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a floating gate electrode.

12. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a stack gate cell.

13. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a split gate cell.

14. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a control gate electrode.

15. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a stack gate cell.

16. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a split gate cell.

20. (Three times amended herein) A method of forming a semiconductor integrated circuit, said method comprising:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities through said gate dielectric layer and into said second region, said halogen-containing impurities formed of a dosage greater than about 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2, said selectively implanting at an implant energy that is about 0.1 keV to about 40 keV; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process.

D1 cont

21. (Three times amended herein) The method of claim 20

wherein said selectively implanting halogen-containing impurities into said first region also includes selectively implanting halogen-containing impurities into said second region such that said first region has a greater halogen concentration than said second region, said halogen-containing impurities in said second region formed of a dosage greater than about 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2.

22. (As filed) The method of claim 20 wherein said halogen containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

23 (As filed) The method of claim 20 further comprising forming a third thickness of dielectric material overlying a third region, said third region being spatially apart from said first region and said second region.

24. (As previously amended) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, said first region directly adjacent said second region;

forming a dielectric layer on said substrate;

masking said dielectric layer to expose said first region;

introducing a halogen-containing impurities through said dielectric layer and into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region,

said oxidizing process comprising a thermal anneal at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

D' cont

25. (As previously added) The method of claim 24 wherein said introducing said halogen-containing impurities comprises an ion implantation.

26. (As previously added) The method of claim 24 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

27. (Three times amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired, a second region where a second oxide layer thickness is desired, and a third region where a third oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region, and a different halogen concentration in said third region than in said first region and said second region, each of said higher halogen concentration and said different halogen concentration; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.

28. (As previously added) The method of claim 27 wherein said performing an oxidizing process also simultaneously forms said third oxide layer thickness at said third region.

D' cont

29. (Once amended herein) The method of claim 6 wherein at least one of said first and second concentrations formed of a dosage of said halogen-containing impurities greater than about 1 x 10^{14} carriers/cm^2 and less than about 1 x 10^{15} carriers/cm^2.

30. (As previously added)The method of claim 20 wherein said forming said first and second thickness of dielectric material comprises an anneal process performed at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

31. (As previously added) The method of claim 30 wherein said anneal process is further performed at a pressure of about 760 Torr.

D2

32. (Added herein) A method of forming a semiconductor device, the method comprising:

providing a substrate having a first region and a second region;

introducing flourine into the substrate to form a higher concentration in the first region than the second region;

placing the substrate in an oxidizing environment, wherein an oxide layer forms on the substrate with a first thickness over the first region and a second thickness over the second region;

in a single step, forming a conductive layer disposed above the first region and the second region; and

removing portions of the oxide layer and the conductive layer to form gate structures disposed over the substrate.

D& conl